

# CCPS Revision B

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## 1. GENERAL

During the use of Thor's power supply, I experienced several times a failure on the Driver PCB:

- the HV trace (560 Vdc) was arcing to a nearby mains trace (phase or neutral)
- two IGBT on the same bridge arm got short-circuited
- the 10A FF fuse blew up
- large portions of the relative PCB traces were vaporized.

Did the IGBT short generate an extravoltage that arced the mains to HV or the other way round? No way to know that...

In January 2002 I decided to revise the whole power supply in order to improve its reliability. This is the (compressed) description of that activity and of its results. In the following I assume that you are familiar with Thor's power supply design and architecture.

## 2. BETTER IMMUNITY TO SPARK GAP TRANSIENTS

The clearance between the HV and mains traces was really too small, about 3 mm. The transients generated by Thor were probably "shaking" the almost floating HV, up to a point where breakdown occurred.

I took the CCPS home and used only a single Driver module (max. 5 kV) to charge an external 0.1 uF capacitor. I short-circuited the capacitor with some 15 cm length of HV wire and took different measurements with a digital scope. I also simulated the same circuit with MicroSim and got similar results (see Figure 1). D1 to D4 are the IGBT bridge freewheeling diodes, V1 and V2 represent the HV supply (560 Vdc).

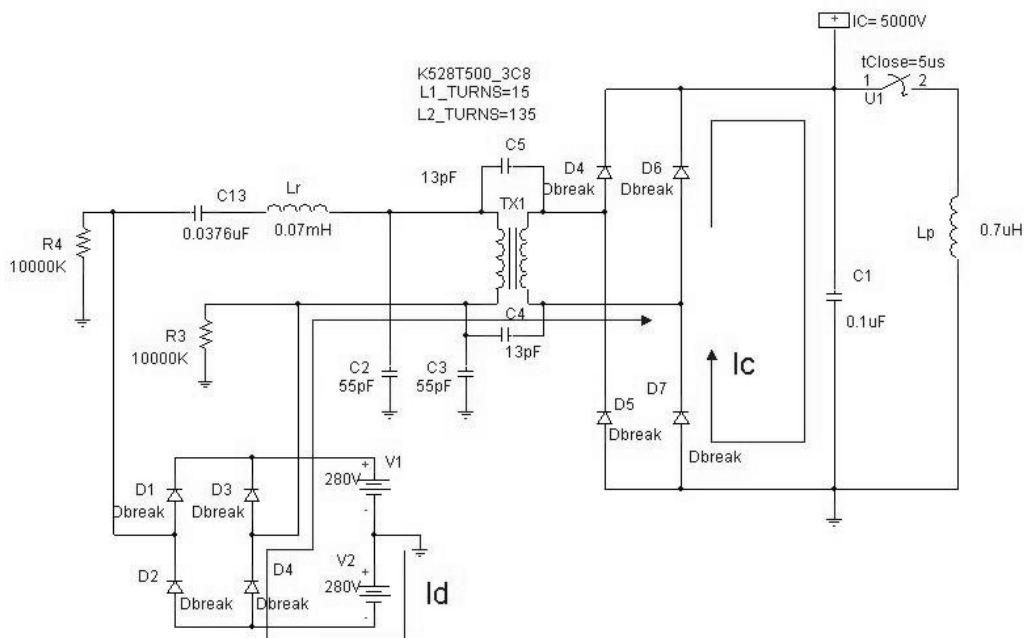


Figure 1 Schematics for the simulation of spark gap transients.

So, what happens? When switch U1 closes, voltage across C1 swings, changes polarity and becomes negative. The bridge made by D4 to D7 is forward biased (current flow  $I_c$ ). The secondary terminals of the transformer TX1 are forced at about at the same (negative) potential. For the TX1

interwinding capacitance (C4 and C5), a fraction of that voltage will reach the primary terminals, that will be virtually short-circuited. Now, D1 to D4 will clip this voltage transient to +280VDC and clamp it to -280VDC in respect to ground (current flow Id). As these diodes are not ideal, the initial transient front will get through and tend to be superimposed to the 560 Vdc.

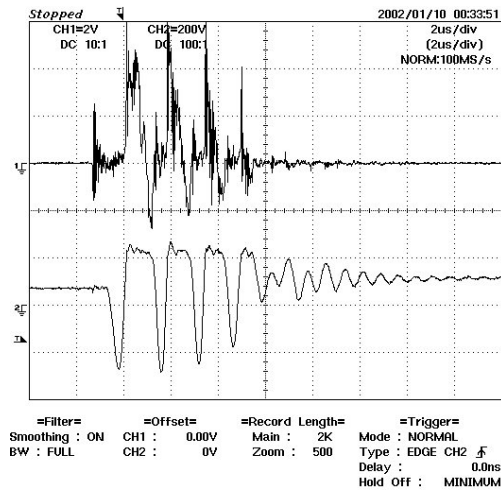


Figure 2 Transient caused by wrong ground wiring.

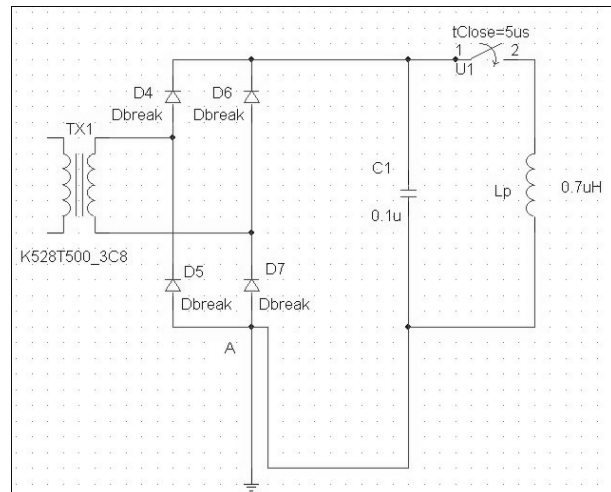


Figure 3 Wrong grounding to node A.

The key point here is that the transient is generated between TX1 primary winding and GND (or 560 Vdc line), not between the two primary terminals of TX1.

After the simulation I measured current and voltage (in respect to GND) of the connection between a primary terminal of TX1 and the anode of D3 (Figure 2):

- trace 1 is the current (2A/div)
- trace 2 is the voltage (200V/div)

This transient train could be observed when the capacitor C1 (charged at 1.2 kV) was shorted. From the waves polarity (I spare you from the details) it was possible to see that charge coming from TX1 was "feeding" the 560 Vdc line, through the flywheel diodes.

With C1 charged at 2 kV the current in the flywheel diodes peaked to 8A! Now imagine what happens when there are 4 Driver modules output in series. The upper one of the chain will see now a 5 kV charged capacitor being shorted (1/4 of the full 20 kV), but this time the module has got a 5 kV DC offset above GND. How much the flywheel diode current might be?

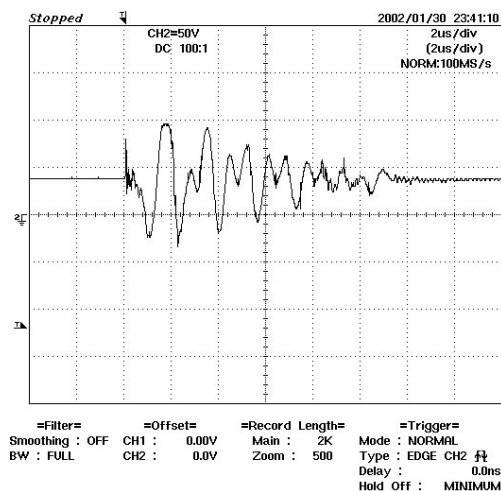


Figure 4 Reduced transients using an improved ground wiring.

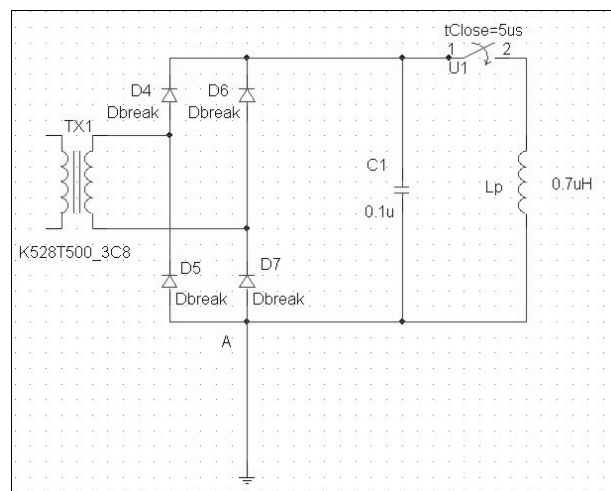


Figure 5 A better grounding to node A.

I have also moved my probes to the other leg of XT1 and measured the SAME waveforms and with the SAME polarity. For these transients, the TX1 primary terminals appeared really as shorted together at the same potential.

Inspecting the Transformer module I noticed that the GND connection of the diode bridge ran parallel to the external capacitor connection for a good 15 cm (Figure 3) before reaching GND. By simply having the wires separated and far from each other I was able to reduce the amplitude of the voltage transient generated to about 100 Vpp (see Figure 4). Then I tried to connect the primary capacitor GND directly to the "solid GND" copper bar: the transient was back, at full amplitude.

Lesson learnt: transients are generated by potential super-imposed to the connection of the HV bridge (node A) to GND.

In the first case, potential was electromagnetically induced in the A-GND net by the C1 grounding wire running parallel. In the second case, when the primary cap was connected to the GND copper bar, potential was created by the capacitor current flowing too through the A-GND net. The stray inductance of the wire generated the voltage rise. Eventually I rewired the connections of the Transformer module under test as from Figure 5, obtaining a final transient as from Figure 4.

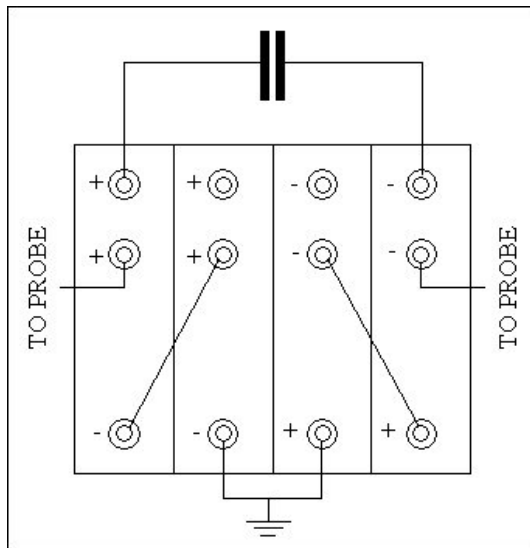


Figure 6 The original Transformer module interconnection scheme.

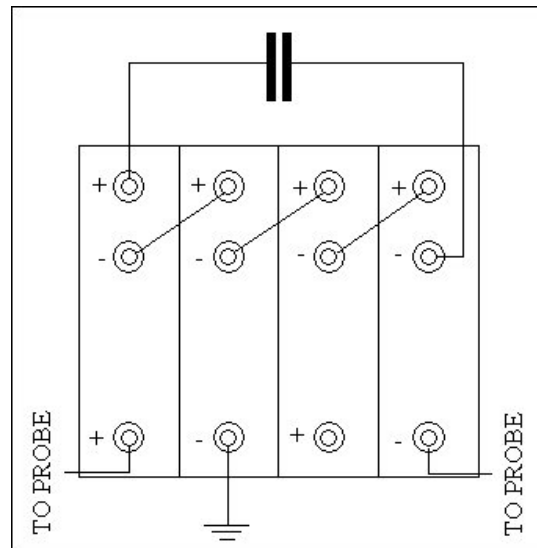


Figure 7 The improved Transformer module interconnection scheme.

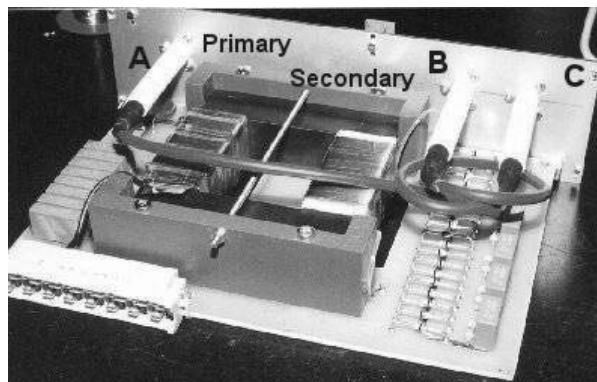


Figure 8 The original Transformer module interconnection scheme.

Back to the full power supply configuration, featuring 4 Drivers and 4 Transformer modules with

outputs connected in series, I used the “lesson learnt” above to improve things. I modified the Transformer module internal and external connections as from Figure 7. Keep in mind that, in each module, the HV diode bridge is always directly connected to the upper two connectors B and C (see Figure 8), while the lower connector A uses about 15 cm of HV cable. It is, therefore, much better to run the capacitor charge/discharge current through the upper connectors than through the lower ones.

After these modifications, short-circuiting a capacitor charged at 1 kV with two modules in series I could measure a transient of only 50 Vpp on the module that was 500 Vdc above ground.

### 3. THE BOOSTRAP PROBLEM

The high-side IGBT Q1 gate drive is fed from a floating power supply constituted by C9 (see the old schematics), while Q3 is fed from C10. These are the so-called “bootstrap” components. The name comes from the fact that C9 and C10 get charged to VP15 only when the low-side corresponding IGBT conducts.

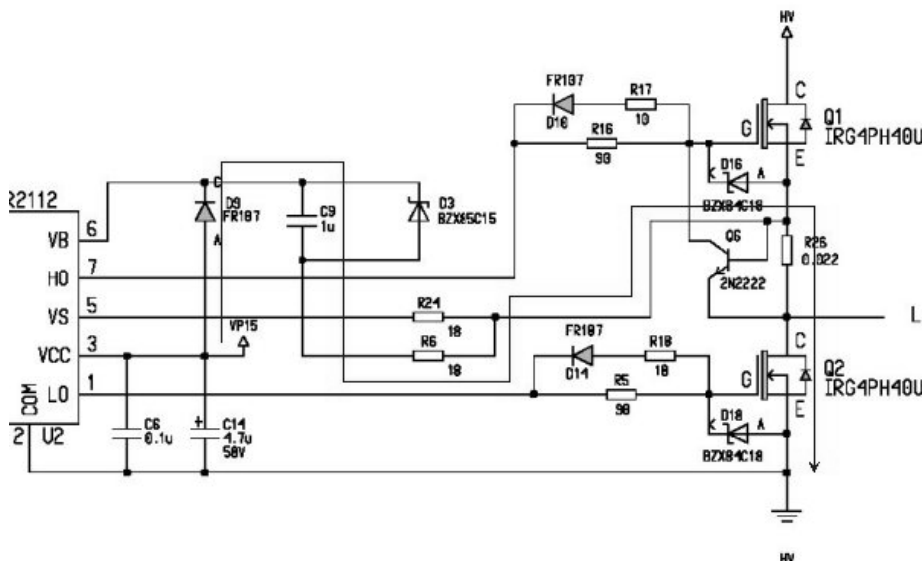


Figure 9 Current flow charging the bootstrap capacitor C9 to VP15.

This is not an issue for a usual switching power supply, where the bridge is switching continuously, but the situation is different for a CCPS, inherently working in discontinuous mode. The first bridge commutations at the capacitor charge beginning (and possibly the sporadic commutations needed to maintain the capacitor charged) will easily fail to switch the high-side IGBTs reliably on, because C9 and C10 are not yet charged at a sufficient voltage.

This effect could be observed quite easily with a digital scope. The drive pulses with insufficient charge reserve resulted in a rapid IGBT on-off cycle that, in turn, generated quite ugly transients. More, the series resonant load drive synchronism was broken: the load was driven with a wrong sequence, resulting in high-current transients in the load itself.

To solve this problem I added the signal ENC, working as an on-off control for the high-side IGBTs. ENA and ENB now control directly the low-side IGBTs, while they control also the high-side IGBTs only if ENC=1 (see Figure 11). This way, ENA and ENB can be made clocking continuously and capacitors C9 and C10 will be kept charged. The resonant load will be powered only when ENC=1.

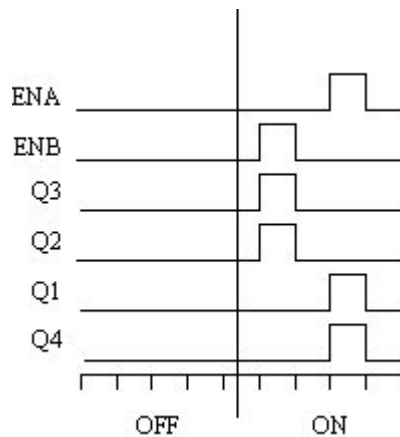


Figure 10 The original drive signals and their effect on IGBT Q1-Q4 switching.

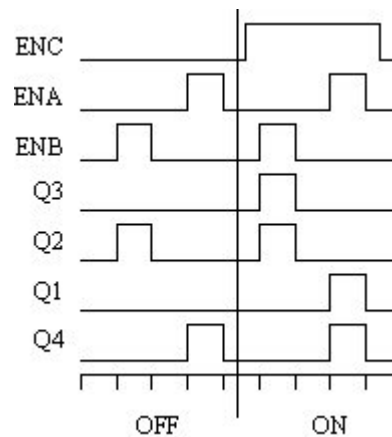


Figure 11 The new drive solution, featuring ENC for enabling the high-side IGBTs.

## 4. MODIFICATIONS TO THE DRIVER MODULE

After having optimized the Transformer modules and their cabling, it was time to examine the Driver module for possible improvements. I made the following changes:

1. The drive signals ENA and ENB experienced crosstalk and were also very prone to EMI. This translated into the possibility of shoot-through. I separated the return wires of ENA and ENB, and modified their input network to allow for RS-422 level drive. On the Controller module, I added an AM26LS31 chip (quadruple RS-422 driver) to provide the required differential drive signals.
2. I added the drive signal ENC (RS-422 levels) for the reason described in the previous chapter. As its use requires modifications also in the Controller module, I added also a jumper to force ENC=1. This way, the new Driver is ready for the new ENC drive mode, but still compatible backwards with the current (old) Controller.
3. I rewired ENA, ENB and ENC on the backpanel, using twisted-pair cable.
4. The 230 Vac transformer used on each module took a lot of space. I added a single toroidal transformer 230 V / 18 V inside the rack and fed all four modules from that. This way I saved space and didn't have anymore mains phase and neutral on the Driver PCB.
5. The gained space allowed me to turn by 90 degrees the IGBT group. The new position allows for easily replacing one or more IGBTs without having to disassemble the four of them
6. I added a connection to the PE (Protective Earth) for EMC filtering.
7. I noticed that the HCPL2430 has got TTL outputs, while the IR2110 has got CMOS inputs. Therefore, I used only HCT logic between them (5V CMOS with TTL inputs). ACT would have been a second choice, but too fast for the job and introducing more risks than benefits.
8. The two big 470 uF 400 V smoothing capacitors, the three mains fuses and the 3-phase bridge did also take a lot of space. I decided to move all of them out of the module and bring the readily rectified 560 Vdc to the PCB. I used stud type capacitors, mounted with the 3-phase diode bridge on an aluminium backpanel very near to the driver DIN connectors, to minimize connection stray inductance.
9. On the Driver PCB I added two 0.33 uF 1 kV pulse capacitors in parallel to the 560 Vdc, very near to the IGBT legs, to provide a reserve for the fastest transients.
10. I also eliminated the fuses (12 in total) on the 3 phases feeding the 3-phase diode bridge. The on-board FF 10A fuse provides already protection and flashover danger is eliminated because mains isn't brought to the PCB anymore. If nothing else helps, the automatic fuse feeding the whole rack opens in case of overload.
11. Return current flowing back from the resonant load through the IGBT flywheel diodes tends to raise the voltage between HV+ and HV- (560 Vdc). I added a 560 Vdc varistor between HV+ and HV- for protection.
12. I reduced the footprint of resistors and diodes to allow for tighter component packing.



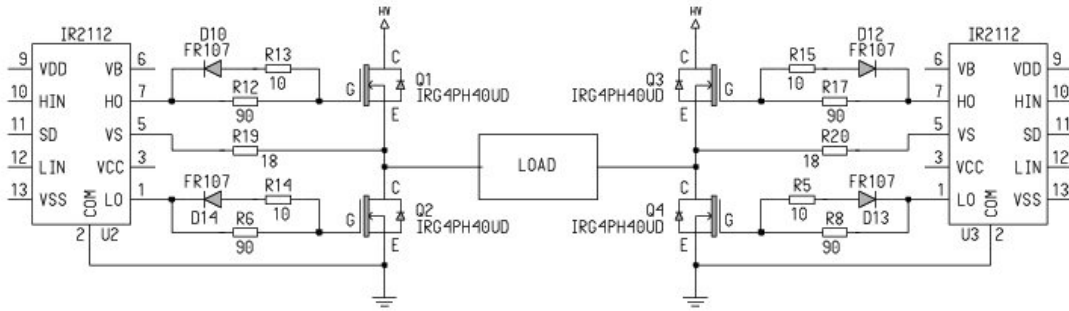


Figure 13 Simplified schematics of the Driver's full-bridge.

### 5.1. Effect of the IGBT reverse transfer capacitance

Without big difficulties I could measure serious transients on the gate of all IGBTs: see Figure 16 and Figure 18, example. These transients appeared in correspondence with the ON/OFF commutation of the paired IGBT on the same side of the bridge and were due to the IGBT reverse transfer capacitance  $C_{rev}$  (in other words, the capacitance between gate and collector). This mechanism is (or should be) well known but a short explanation is still in place.

The first case is when  $V_{ce}$  grows rapidly. Referring to Figure 14, when Q2 (the aggressor) starts conducting,  $V_{ce}$  of Q1 (the victim) increases tending to HV. The capacitance  $C_{rev}$  charges (to  $HV - V_g$ ) with current  $I_c$  through the gate resistance R. This current generates a potential  $V_r$  on R that adds to the original gate drive  $V_g$ . Therefore, the net result of Q2 commutating on is a positive transient on the gate of Q1.

The second case is when  $V_{ce}$  decreases rapidly. Referring to Figure 15, when Q3 (the aggressor) stops conducting,  $V_{ce}$  of Q4 (the victim) decreases tending to zero. The capacitance  $C_{rev}$ , which is charged to  $HV - V_g$ , discharges through R with current  $I_c$ . This current generates a potential  $V_r$  on R that subtracts to the original gate drive  $V_g$ . Therefore, the net result of Q3 commutating off is a negative transient on the gate of Q4.

In a nutshell, whatever is the gate state of the victim IGBT, a rapid change of its  $V_{ce}$  will tend either to turn it on or off.

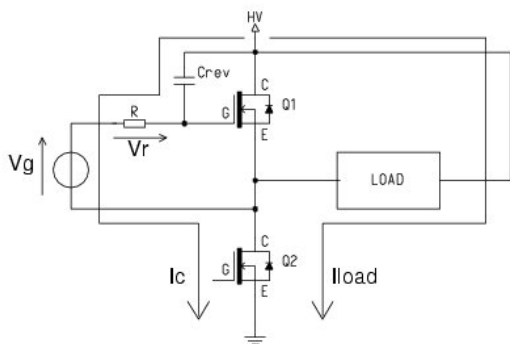


Figure 14 Q2 closing generates a positive transient on Q1 gate.

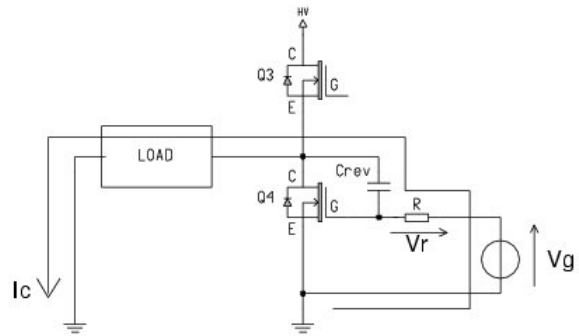


Figure 15 Q3 opening generates a negative transient on Q4 gate.

The natural solution to the above problem is to provide a low impedance gate drive: decreasing the value of R also the transient  $V_r$  gets reduced. In particular, as the victim IGBT is always attacked when in off state, a low off-state impedance is required. I modified the gate drive networks as follows:

- on all four IGBTs, I replaced the series of the FR107 and the 10-ohm resistor with a single PRL5819 SMD schottky diode.
- On the high-side IGBTs, I also replaced the 18-ohm resistors (R19 and R20) with a short.

The improvement achieved by implementing this technique can be easily seen from Figure 17 and



Figure 19.

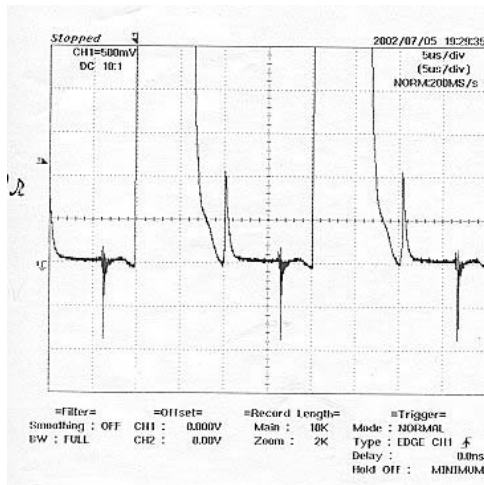


Figure 16  $V_{ge}(Q1)$  with  $R19 = 18 \text{ ohm}$ .

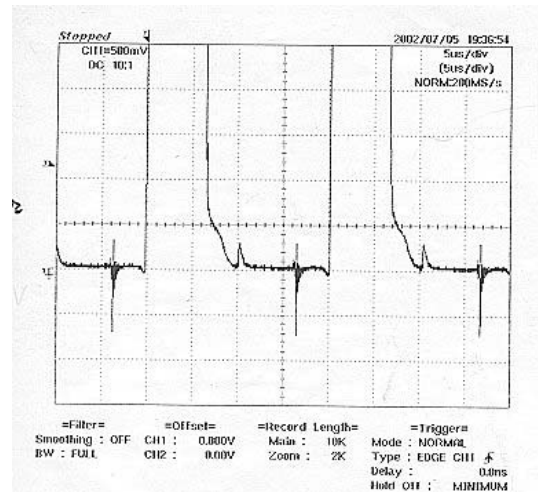


Figure 17  $V_{ge}(Q1)$  with  $R19 = 0 \text{ ohm}$ .

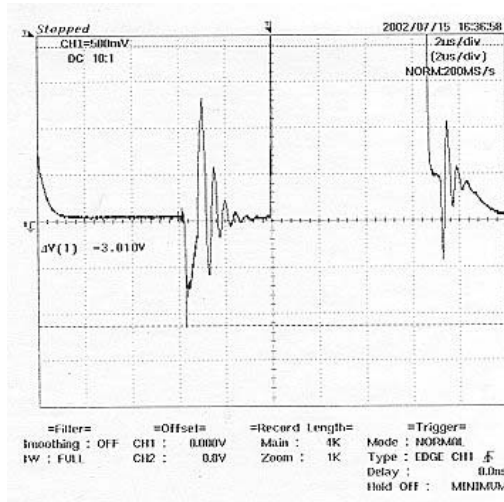


Figure 18  $V_{ge}(Q4)$  with  $R8 = 90 \text{ ohm}$ .

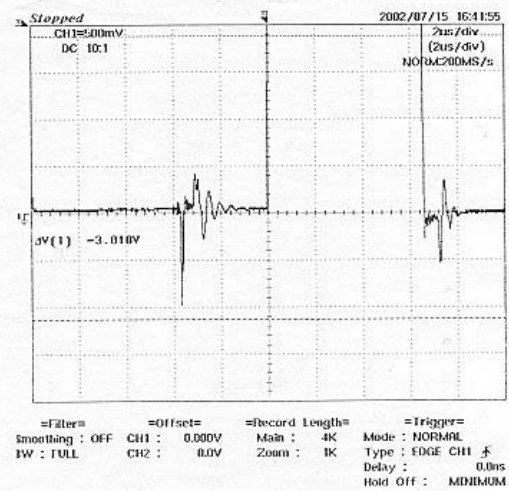


Figure 19  $V_{ge}(Q4)$  with  $R8 = 0 \text{ ohm}$ .

## 5.2. Driver IC VS undershoot

Being satisfied with the resistive load, I started using an inductive one. I added a coil made of some 20 turns of air-wound wire in series with the same 10-ohm power resistor. HV was again fed with 30 Vdc.  $V_{ge}$  of the IGBTs looked good but I measured a dangerous undershoot of about  $-7 \text{ V}$  (Figure 21) on the VS pin (pin 5) of the IR2112 driver IC in correspondence of the load being turned off.

On the IR2112 datasheet are mentioned several restrictions regarding the potential that can be applied to VS. In a nutshell, voltages lower than  $-5 \text{ V}$  will trigger a mechanism internal to the IC that will temporarily latch the high side output in its current state and will not respond to input transitions (on the high-side) while the undershoot persists. Voltages lower than  $-10 \text{ V}$  could actually damage the chip.

The transients I measured were generated as follows. Refer to Figure 20. When Q1 and Q4 are conducting, current  $I_{load}$  flows through the load. When both of these IGBT turn off, the inductive load will generate an opposite polarity voltage upon its terminals, trying to sustain a current with the same direction. The resulting current  $I_{rev}$  will have no other possibility than to flow through the flywheel diodes integrated with IGBTs Q2 and Q3. Once VS falls 2 V or so below ground, the diode of Q2 is supposed to clamp the node to ground. Actually, VS falls way below ground until the diode gets through its forward recovery process and the current overcomes the effect of the parasitic inductances.

The solution for this problem in the Driver V 5.0 and its previous versions had been an 18-ohm

resistor (R19) between the IR2112 VS pin and the load node, but I had already found out (see previous chapter) that this was prone to generate transients on the IGBT gates. What I needed was a compromise between a 0 and 18 ohm solution: I decided to use a fast diode directly between pin VS and ground, plus a small value for R19. The diode had to have the following characteristics:

- low forward drop voltage
- at least 600 V of continuous reverse voltage
- low forward recovery time
- SMD case to limit the lead inductance

A schottky diode was suppressing perfectly the transient: unfortunately the reverse voltage constrain made it unviable. I tested several diodes with very low reverse recovery time (e.g. 30 ns): sadly, they had a forward recovery time of several hundreds of nanoseconds. I tested also some diodes with guaranteed low forward recovery time: being in big through-hole packages made cumbersome their connection to the IR2112 and, actually, lengthened their recovery time.

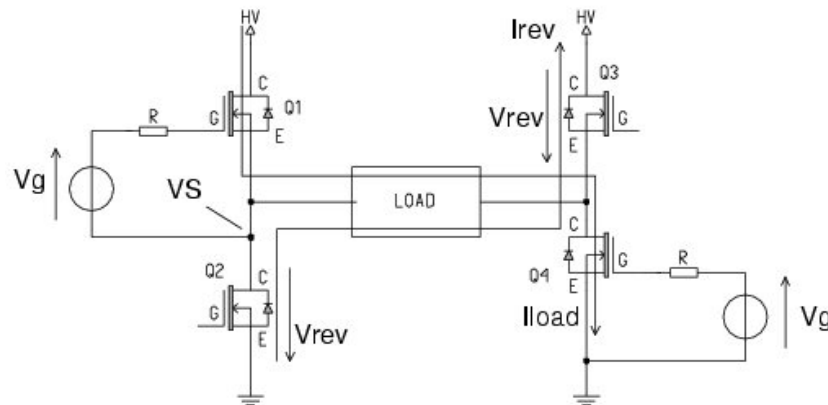


Figure 20 When Q1 and Q4 turn off, a negative transient is generated on node VS.

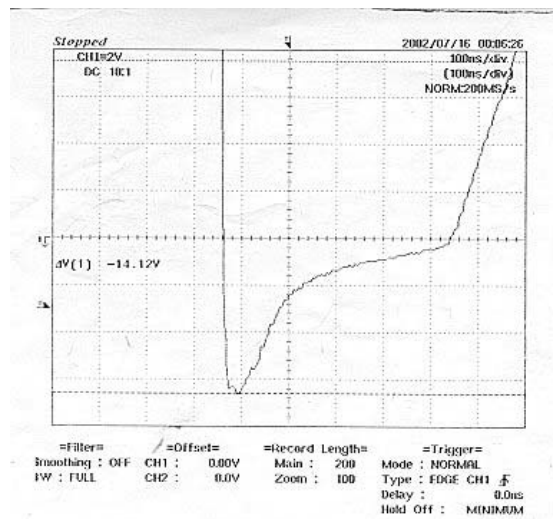


Figure 21 VS undershoot with R19=0 ohm.

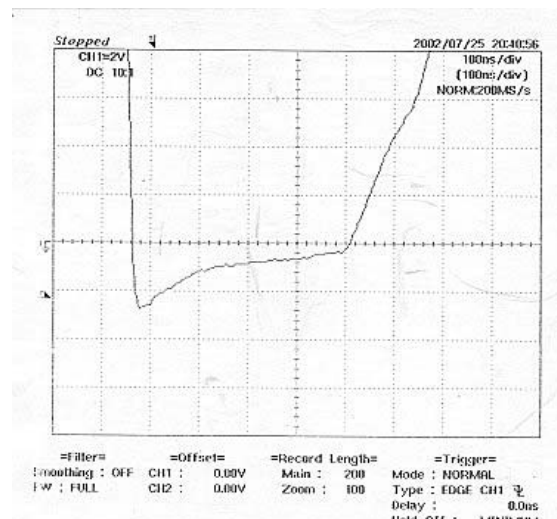


Figure 22 VS undershoot with R19=4.7 ohm and diode BYG70J.

Eventually the best candidate was the fast soft-recovery, controlled avalanche rectifier BYG70J with:

- forward drop voltage of 2.1 V
- continuous reverse voltage of 600 V, avalanche breakdown at 700 V
- reverse recovery time of 30 ns

- DO-214 case

I replaced the 18-ohm carbon R19 with 4.7-ohm thick film SMD resistor and connected the diode of from Figure 23. My measured transient got reduced to some  $-2.8\text{ V}$  (Figure 22).

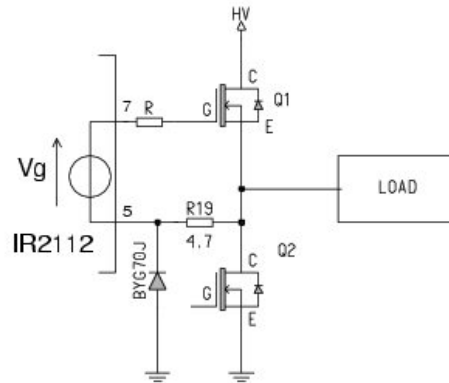


Figure 23 Preventing negative transients on pin 5 (VS).

### 5.3. The stray inductance strikes back

After having optimized with both a resistive and an inductive load, it was time to check all over again with the real load, at a respectable high working voltage. I connected a Transformer board as the Driver load and fed HV with 300 Vdc. I measured a VS undershoot safely within limits, while  $V_{ge}$  of the IGBTs didn't show serious transients when driving an off state.

On the contrary,  $V_{ge}$  was not "clean" when driving an on-state: an ugly ringing was present in correspondence of  $V_{ge}$  reaching the Miller plateau (Figure 25). The same ringing could be measured in the resonant load and several nodes of the Driver. By reducing HV to zero I was able to verify that the transient disappeared (Figure 24), which confirmed the IGBT emitter stray inductance being responsible for the transient.

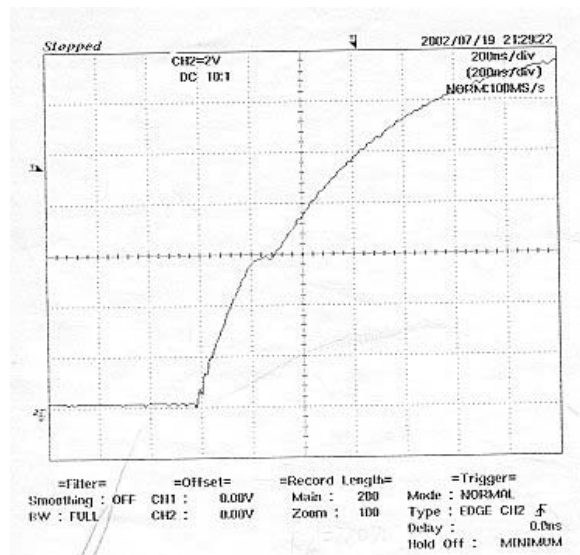


Figure 24  $V_{ge}(Q2)$  with  $R6 = 90\text{ ohm}$  and  $HV = 0\text{ V}$ .

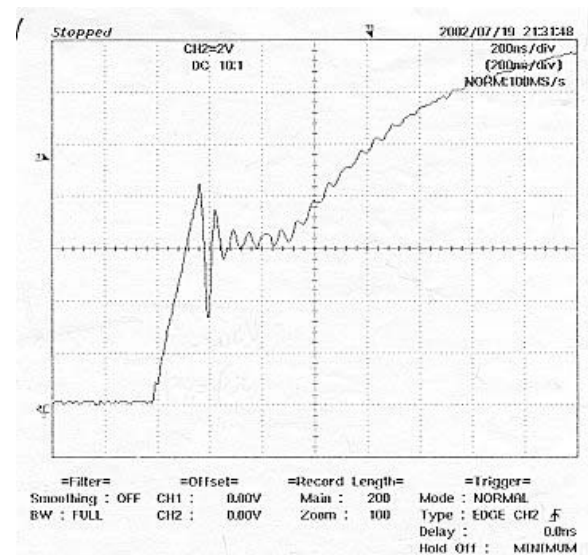


Figure 25  $V_{ge}(Q2)$  with  $R6 = 90\text{ ohm}$  and  $HV = 300\text{ V}$ .

The emitter stray inductance is the sum of the IGBT internal bond wire, the package lead and the connecting trace inductances. It affects the switching behaviour with two mechanisms. First, as the gate charging current must flow also through this inductance, the resulting potential drop slows down the charging. Second, the emitter inductance creates a negative feedback between load and gate current. As the load current increases, again, a voltage is developed upon the inductance that subtracts to the gate drive voltage. The rate of the gate charging is, once again, decreased. More, the emitter inductance

forms together with the IGBT internal capacitance  $C_{ies}$  a resonant circuit that is excited by the steep edges of the gate drive voltage. This is the cause of the ringing that can be seen in Figure 25 and Figure 27.

On the other hand, a slow turn-on increases the IGBT commutation losses. Referring to Figure 26, during the first  $V_{ge}$  rising ( $t_1$ ), before of the Miller plateau,  $V_{ce}$  stays almost constant and the load current increases. During the following phase, the Miller plateau  $t_2$ , the load current stays constant and  $V_{ce}$  drops down to almost zero. Of course, this is an idealized situation with a resistive load but, in a nutshell, commutation losses are experienced from the first application of  $V_{ge}$  until the end of the Miller plateau.

Aware of the above issues, I decided to trade the danger of these nasty transients propagating all around the Driver circuitry against an increased IGBT thermal dissipation. I tested several values for the gate resistor  $R_6$  of  $Q_2$ . For instance, I measured a turn-on time of 260 ns without gate resistor (Figure 27) and of 540 ns with the current 90-ohm value (Figure 25). I eventually selected 220 ohm, resulting in well damped oscillations and a turn-on time of about 1100 ns.

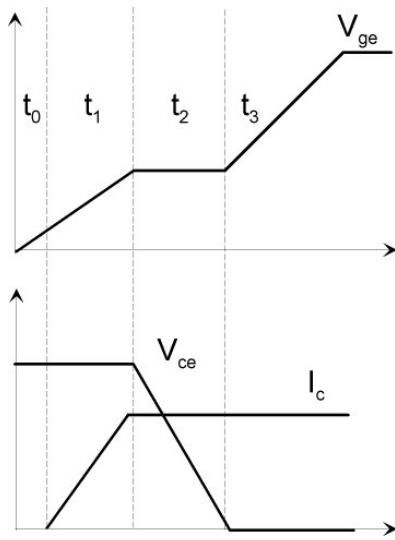


Figure 26 Idealized turn-on IGBT switching.

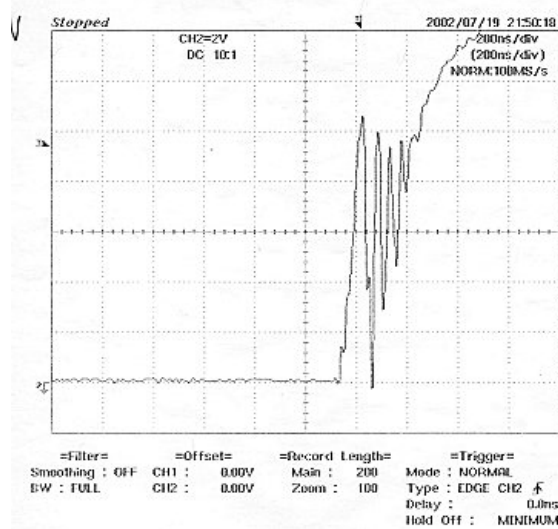


Figure 27  $V_{ge}(Q_2)$  with  $R_6 = 0$  ohm and  $HV = 300$  V.

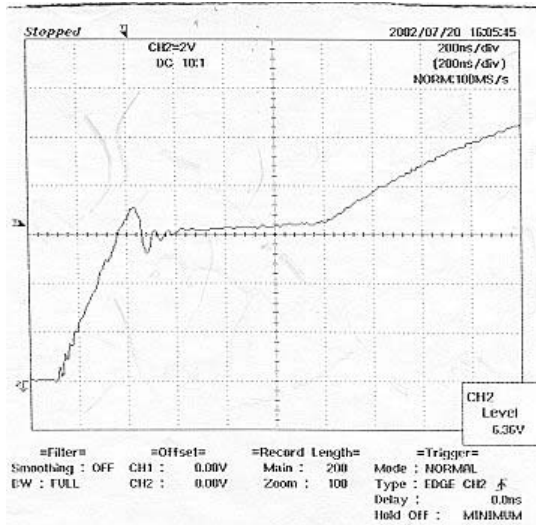


Figure 28  $V_{ge}(Q_2)$  with  $R_6 = 220$  ohm and  $HV = 300$  V.

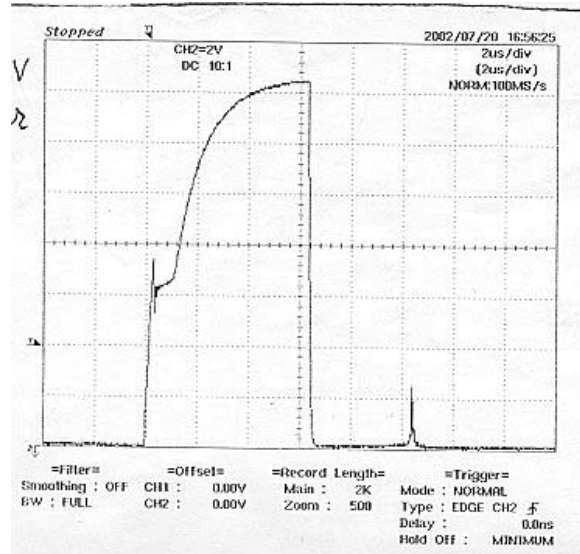


Figure 29  $V_{ge}(Q_2)$  with  $R_6 = 220$  ohm and  $HV = 390$  V.

## 6. CONCLUSION

I implemented the modifications listed in the previous chapter directly on the V 5.0 PCB, without designing a new one. I also updated the schematics and marked them as V 7.0 (see Figure 30). At today (December 2002), I haven't yet experienced failures of any kind. On the other hand, I must admit that I have been running Thor only a few times. Time will show if this group of modifications has actually generated a more robust design or not.

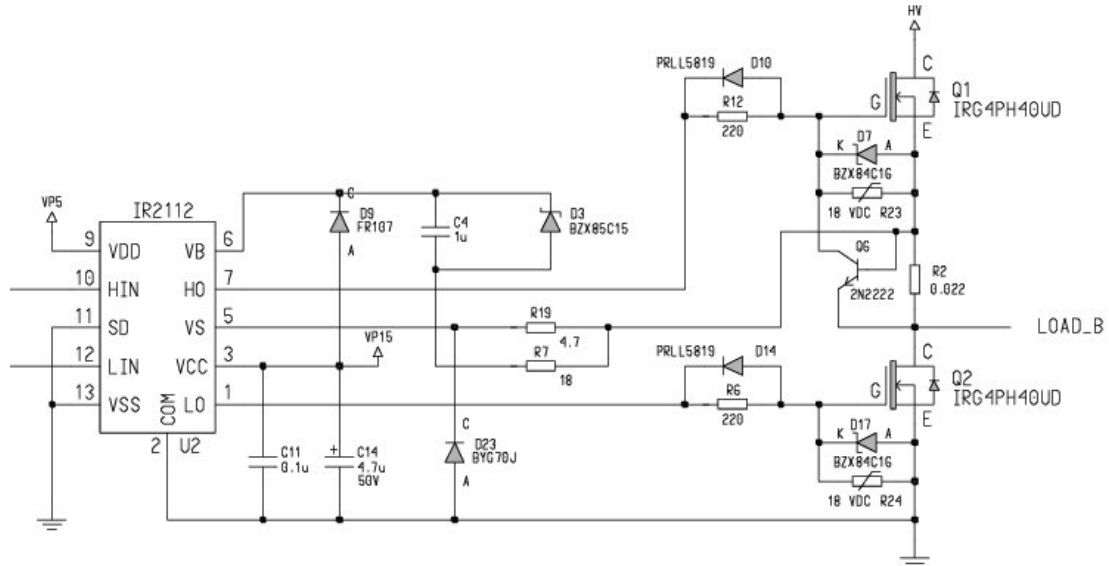


Figure 30 Driver V 7.0 (one side of the IGBT bridge).